IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A process of testing spacing of wiring in a circuit comprising:

forming a plurality of conductor rectangles representative of conductors of said circuit;

forming minimum spacing rectangles around said plurality of conductor rectangles, said minimum spacing rectangles being larger than respective ones of said plurality of conductor rectangles;

identifying a possible error rectangle when a first conductor rectangle of said plurality of conductor rectangles occupies a portion of a minimum spacing rectangle of a second conductor rectangle of said plurality of conductor rectangles;

checking whether said possible error rectangle is a true error; and

reporting said true errors.

2. (Previously Cancelled).

3. (Currently Amended) The process in claim 1, wherein said forming minimum spacing rectangles comprises forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said plurality of conductor rectangles.

4. (Original) The process in claim 1, wherein said conductors are within a single net.

5. (Original) The process in claim 1, wherein said circuit comprises a plurality of nets and said process further includes checking for shorts between different ones of said nets.

6. (Original) The process in claim 1, further comprising dividing said possible error rectangle into at least two possible error rectangles if said possible error rectangle is partially covered by a third conductor of said conductors.

7. (Currently Amended) A process of testing spacing of elements in a structure comprising:

forming a plurality of element rectangles representative of elements of said structure;

forming minimum spacing rectangles around said plurality of element rectangles, said minimum spacing rectangles being larger than respective ones of said plurality of element rectangles;

identifying a possible error rectangle when a first element rectangle of said plurality of element rectangles occupies a portion of a minimum spacing rectangle of a second element rectangle of said plurality of element rectangles;

checking whether said possible error rectangle is a true error; and

reporting said true errors.

8. (Previously Cancelled).

9. (Currently Amended) The process in claim 7, wherein said forming minimum spacing rectangles comprises forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said plurality of element rectangles.

10. (Original) The process in claim 7, wherein said elements are within a single net.

11. (Original) The process in claim 7, wherein said structure comprises a plurality of nets and said process further includes checking for shorts between different ones of said nets.

12. (Original) The process in claim 7, further comprising dividing said possible error rectangle into at least two possible error rectangles if said possible error rectangle is partially covered by a third element of said elements.

13. (Currently Amended) A computer system for testing spacing of wiring in a circuit comprising:

a unit for forming a plurality of conductor rectangles representative of conductors of said circuit;

a unit for forming minimum spacing rectangles around said plurality of conductor rectangles, said minimum spacing rectangles being larger than respective ones of said plurality of conductor rectangles;

a unit for identifying a possible error rectangle when a first conductor rectangle of said plurality of conductor rectangles occupies a portion of a minimum spacing rectangle of a second conductor rectangle of said plurality of conductor rectangles;

a unit for checking whether said possible error rectangle is a true error; and

a unit for reporting said true errors.

14. (Previously Cancelled).

15. (Currently Amended) The computer system in claim 13, wherein said unit for forming minimum spacing rectangles comprises a unit for forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said plurality of conductor rectangles.

16. (Original) The computer system in claim 13, wherein said conductors are within a single net.

17. (Original) The computer system in claim 13, wherein said circuit comprises a plurality of nets and said computer system further includes a unit for checking for shorts between different ones of said nets.

18. (Original) The computer system in claim 13, further comprising a unit for dividing said possible error rectangle into at least two possible error rectangle if said possible error rectangle is partially covered by a third conductor of said conductors.

19. (Currently Amended) A computer program product comprising a program storage device readable by a computer system tangibly embodying a program of instructions executed by said computer system to perform a process for testing spacing of wiring in a circuit, said process comprising:

forming a plurality of conductor rectangles representative of conductors of said circuit;

forming minimum spacing rectangles around said plurality of conductor rectangles, said minimum spacing rectangles being larger than respective ones of said plurality of conductor rectangles;

identifying a possible error rectangle when a first conductor rectangle of said plurality of conductor rectangles occupies a portion of a minimum spacing rectangle of a second conductor rectangle of said plurality of conductor rectangles;

checking whether said possible error rectangle is a true error; and

reporting said true errors.

20. (Previously Cancelled).

21. (Currently Amended) The computer program product in claim 19, wherein said forming minimum spacing rectangles comprises forming said minimum spacing rectangles to have sides which are a minimum spacing design constraint distance from sides of respective ones of said plurality of conductor rectangles.

22. (Original) The computer program product in claim 19, wherein said conductors are within a single net.

23. (Original) The computer program product in claim 19, wherein said circuit comprises a plurality of nets and said process further includes checking for shorts between different ones of said nets.

24. (Original) The computer program product in claim 19, said process further comprising dividing said possible error rectangle into at least two possible error rectangle

if said possible error rectangle is partially covered by a third conductor of said conductors.

Please add the following new claims:

25. (New) The method in claim 1, further comprising classifying said possible error rectangle as one of non-diagonal and diagonal.

26. (New) The method in claim 1, wherein said checking process comprises determining if said possible error rectangle is covered by metal.

27. (New) The method in claim 1, wherein said checking process determines that said possible error rectangle is not a true error if said possible error rectangle is entirely covered by metal.

28. (New) The method in claim 1, wherein said checking process determines that said possible error rectangle is not a true error if at least two adjacent sides of said possible error rectangle are covered by metal.